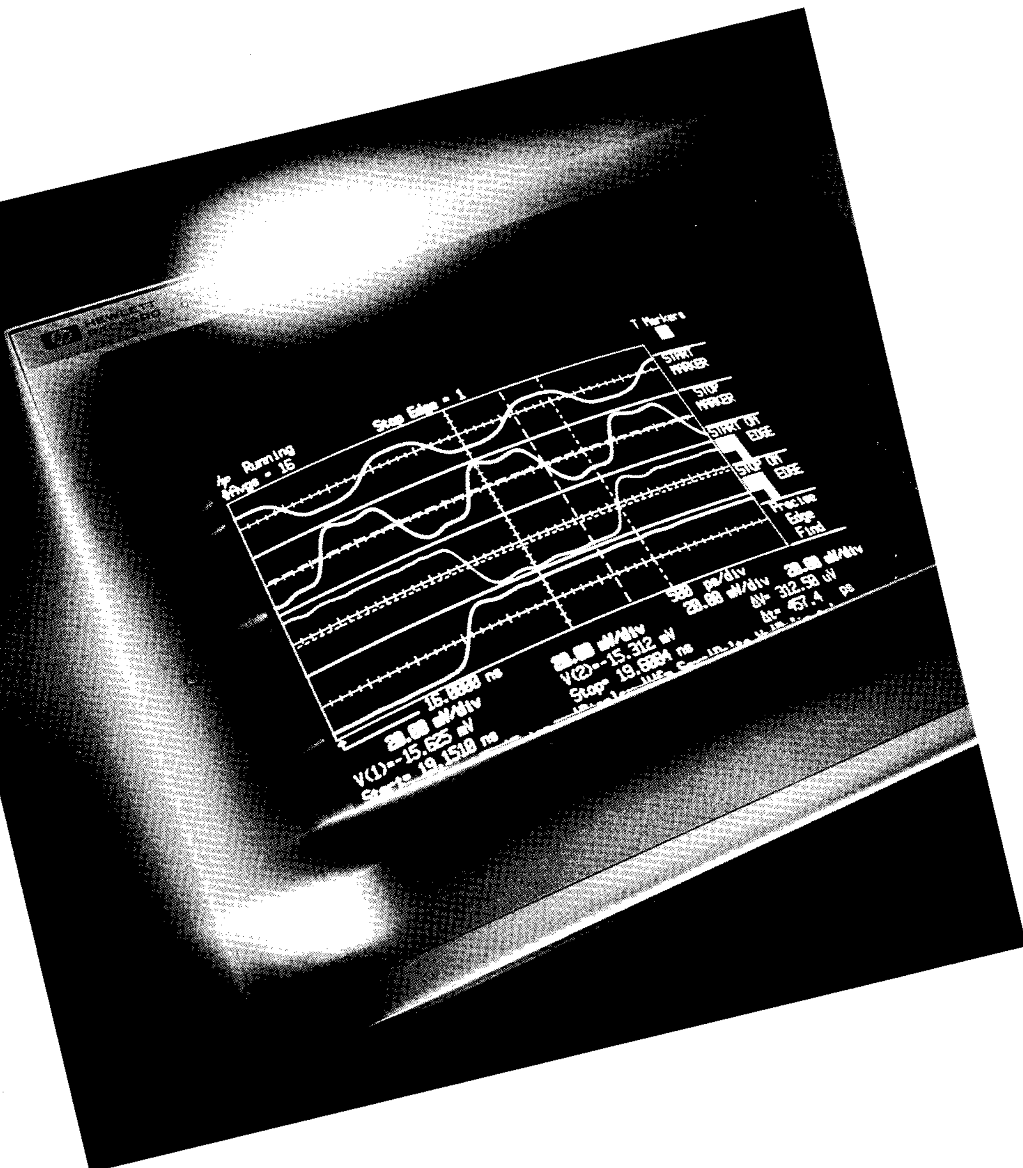
HEWLETT PACKARD

Correlation of Timing Measurements

Application Note 398-2



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Introduction

When comparing test results taken on the bench with a high performance oscilloscope and data taken with a digital test system, quite often the questions arise like: Why does the data not match? Where are all the errors coming from?

This paper describes the phenomena associated with testing high speed devices on a high performance test system and provides a procedure to correlate measurement data.

The systematic limits for measurement accuracy are given by the test system's AC and DC specifications.

Definition: Edge placement accuracy is the worst case deviation of actual value from programmed value.

Consider a typical propagation delay measurement where two timing edges are involved: One edge drives the "clock" input of the part, the other is strobing the output data of the part. Therefore, the placement error of the drive edge, the placement error of the strobe (compare) edge and the drive to receive offset (round trip error) contribute to the measurement error:

  placement accuracy drive
+ placement accuracy strobe
+ drive to receive offset

= measurement error

In case of a set up/hold time measurement which is related to two input edges, the systematic measurement error changes to:

  placement accuracy of drive a
+ placement accuracy of drive b

= measurement error

Besides the edge placement error, the DC accuracy has to be taken into account which determines the worst case deviation of actual drive levels and compare thresholds from programmed values.

Note: This assumes that the DUT is "perfect", which means: does not interfere with the tester.

2. Error Terms due to Interfacing

The device under test (DUT) provides both the AC and the DC loads for the tester. Conversely, the tester output provides the load for the DUT

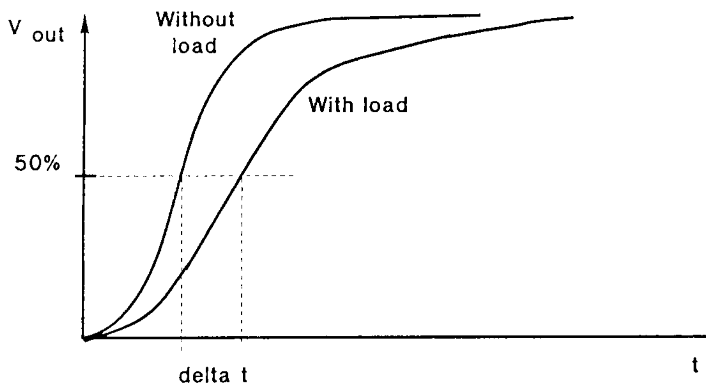


Figure 1. Capacitive loading of tester output

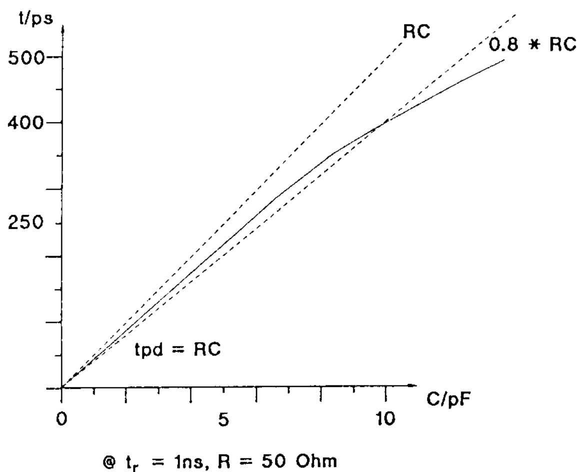


Figure 2. Timing error as function of RC time constant

2.1 AC Loading of Tester Output by DUT

The input capacitance of the DUT and the pin driver's output impedance, which is in general matched to the line impedance of the system, act as a low pass filter thus degrading the effective slewrate the higher the load is.

The resulting timing error (additional delay) is dependent on the intrinsic risetime of the source and the resulting RC time constant.

As a rule of thumb, the timing error at the 50% reference point is:

delta tpd = $0.8 * Z_L *$ delta C

This equation is valid in case of small values of RC.

Example:

Z_L = 50 Ohm

delta C load = 10 pF

=> delta tpd = approx. 400 ps!

2.2 DUT Input Threshold Versus Actual Tester Drive Levels

Test System timing calibration is referenced to the 50% point of the drive signal. In case the input threshold of the DUT differs from this point, a timing error comes into play which is given by:

$$\text{delta t} = \frac{\text{delta voltage (vth-vref)}}{\text{slewrate of drive signal}}$$

Example:

If you apply v_{ie}=OV, v_{ih}=5V to a TTL device, the Test System is referenced to 50% of this 5V swing:

$$v_{ref} = 2.5V$$

Actual TTL threshold is:

$$v_{th} = 1.4V$$

This leads to a timing error of:

$$\text{delta t} = \frac{\text{delta v}}{\text{slewrate}}$$

$$= \frac{2.5v - 1.4v}{2v/ns}$$

$$= 550ps$$

The input circuit as well as additional loads may also bias the tester outputs thus changing the actual drive conditions.

Whereas the bias current (Ib) in most practical cases (CMOS, ECL) may be negligible because of the low source impedance, an ohmic load, e.g. a resistive divider scope probe (500 Ohms or 1000 Ohms), cannot. So a timing error is introduced which is directly proportional to the DC level change with respect to the DUT input threshold. (see figure 3.)

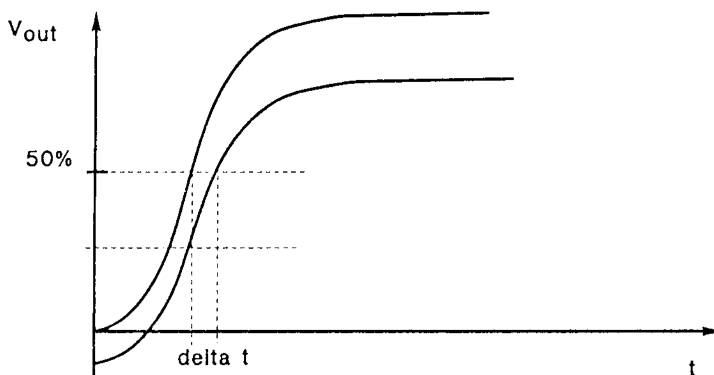


Figure 3. Timing error introduced by level change

2.3 DUT Output AC Loading by Tester

For highest accuracy at high speeds the terminated environment is mandatory (termination at receivers plus resitive divider). This technique reduces the capacitive loading to a minimum (about < 10pF) and provides an ohmic (DC) load instead.

(see App.Note "Testing High Speed Devices")

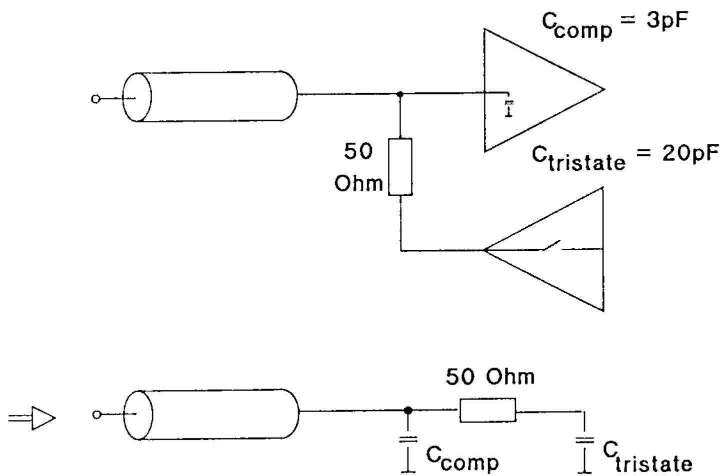


Figure 4. Timing error due to tristate capacitance

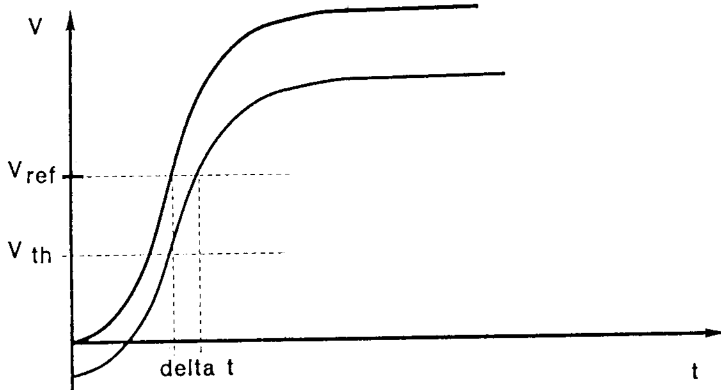
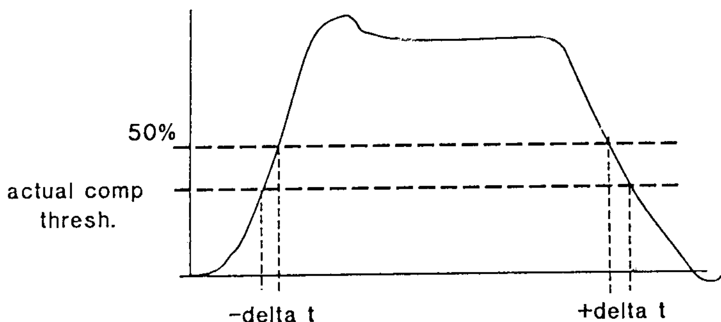


Figure 5. Timing error due to DC offset of comparator threshold



If instead operation into an open (High Z) environment is considered, besides the danger of reflections, the High Z (tristate) capacitance C_{trist} of the pin electronics introduces a low pass filter adding a timing error.

The resulting timing error can be calculated analog to chapter 2.1 with

$$\text{delta t} = 0.8 \times Z_L \times C_{trist}$$
$$= 0.8 \times 50\ \text{Ohm} \times 20\ \text{pF)}$$
$$= 800\text{ps}$$

2.4 DC Threshold Considerations

If tester comparator threshold reference differs from DUT timing reference, a timing error is introduced which is proportional to the voltage difference and the DUT output slewrate:

$$\text{delta t} = \frac{\text{delta v}}{\text{slewrate (DUT)}}$$

DC tolerances e.g. comparator threshold errors and termination voltage errors affect timing accuracy in the same way.

Note: A DC offset of the comparator threshold leads to different propagation delay readings for positive and negative going output edges! (see Fig. 6)

2.5 DUT Wiring

DUT wiring which differs from where the cal reference was taken have to be considered for subnanosecond accuracy. Any interconnect introduces a prop delay proportional to its length. On standard FR4 PCB's, the velocity of signals is about 15 cm/ns (0.5 foot/ns).

A rule of thumb:
1 cm = 66 ps for a trace on PCB.

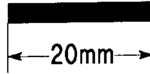


Figure 7. This trace is equivalent to 135ps!

2.6 DUT Specifics

Whereas the tester views all active vectors when it performs e.g. a prop delay test, a scope only sees a few vectors which might not be the device's worst case condition.

A scope needs repetitive patterns, the tester takes measurements in single shots. This can affect the thermal conditions (CMOS, GaAs), which in turn can change timing performance of the part.

Parts typically tend to have different prop delays for rising and falling transitions because of different transition times and internal offsets.

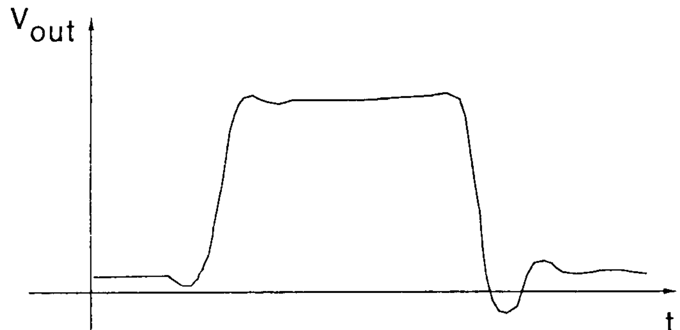


Figure 8. Typical TTL output waveform

3. Correlation Procedure

From the summary of the various associated interfacing error terms and their values it becomes very obvious that they have to be ruled out carefully to get precise measurement results.

3.1 Calibration

The first step is to calibrate the equipment.

The HP82000 system offers three different calibration options:

1. Standard AC Cal

   => +/- 500 ps (D200):

With the standard AC calibration any parameter can be changed:
- data formats
- timing (LE,TE)
- period
- driver levels
- threshold
- pattern.

The error terms for this option are given by the environment temperature and humidity, crosstalk between the channels, jitter of the master clock, master clock accuracy, non-linearity of the delay circuit and by the ageing of the system.

2. Standard AC Cal at test period
   => +/- 350 ps (D200)

With the standard AC calibration at test period the following parameters might/must not be changed:

Parameter not to change:
- period

Parameters to change:
- data formats
- timing (LE, TE)
- driver levels (*)
- thresholds
- pattern.

Fixing to one period setting eliminates the frequency dependency of the system.

3. User AC Cal
   => +/- 250 ps (D200)

With the user calibration we can achieve the best accuracy. Parameters to change / not to change are:

Parameters not to change:
- period
- timing (LE, TE)
- data formats
- driver levels (*)

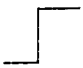
Parameters to change:
- pattern
- thresholds.

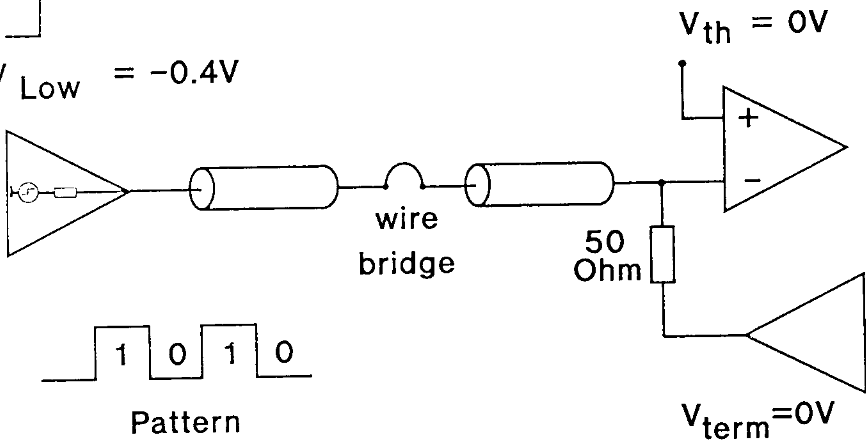
Note: User calibration tunes the system for one specific timing setting, so in case of search functions those pins used for searching should not be included in user cal.

Make sure that your reference oscilloscope is calibrated (AC and DC), too.

3.2 Eliminate System Roundtrip Error Term

Replace your device under test (DUT) by a short piece of wire connecting your reference input (e.g. clock input) with the output under test. Set up the following simple test:





Read "prop delay" of this simple test and enter this reading in the PIN ATTRIBUTES file for SATR. Download this file to hardware and check the "prop delay" once again.

The SATR adds a virtual common delay between drive and receive path, thus compensating for the reading offset for a prop delay measurement.

3.3 Compensation for Capacitive Load

In case the input capacitance is well known, a compensation value for the loading effect can be calculated according to formula,
delta tpd = 0.8 Z_i delta C
and added to the SATR entry.

In case the capacitance is not known, the risetime degradation of the drive signal due to the DUT input loading should be measured with the scope. The timing delta at the 50% reference level can then be entered in the SATR field.

Note: Take into consideration that the scope itself adds some capacitive loading. So for precise comparisons keep the probe always hooked up all the time
(or compensate for the C of the probe tip).

3.4 Input Level Considerations

Verify that you reference your scope measurement to actual levels present at the inputs of the DUT under test to rule out any DC offsets or DC loading effects. Keep the probe hooked up to the test system to maintain loading conditions. Compensate for DC loading of probe by adjustment of drive levels.

3.5 Device Output DC Loading

In case of a terminated environment, the tester comparator "sees" a true image of the signal you can observe at the output of the DUT with the scope. So no additional correction is necessary.

In case of an unterminated environment, the signal will be distorted due to reflections from the open end. Besides that the additional tristate capacitance has to be taken into account.

3.6 Comparator Reference Adjustment

As discussed in chapter 2.4, any DC offset causes timing errors. In order to compensate for these, it is important to " calibrate" the scope view on what the tester "sees". A means of doing that is to perform a dynamic V_{oh}/V_{ol} test (output voltage sensitivity). Read out these values and center the comparator reference setting to 50% point of these values. Read the same values with the scope and set the scope level marker to 50% of scope reading. This method eliminates the DC offsets. Again it is necessary to keep the probe of the scope hooked up all the time so that the loading conditions for the DUT remain constant.

3.7 DUT Specifics

If your scope reading and the test results from the test system are not matching closely after this procedure, you should verify whether the differences are related to DUT specifics.

1. Thermal effects: Especially in CMOS applications, thermal effects may have to be considered. Hence the scope requires a repetitive trigger, you will run the part in a continuous loop to perform your scope measurements. In contrast to that, the test system performs its measurements in single shots. This can cause a temperature difference between both measurements affecting the timing performance. Heat up or cool down the part and observe the behavior of the part on the scope. An "extension" of the single shot measurement by adding a long dummy init loop with the sequencer can also help to approach similar test conditions.

2. The scope "sees" only a small portion of your vector range: To eliminate any effects due to transitions which are not in your view, mask out all other transitions by use of the word mask/pin mask.

4. "Golden" Device Adjustment

An alternate method to eliminate timing offsets is to use one DUT which has been thoroughly evaluated, e.g. on the bench with a scope, and adjust the test system to it. Now, this part becomes your "calibration" reference or your "golden" device.

4.1 Threshold Adjustment

Go through the same procedure as per chapter 3.6 to eliminate the threshold offset of the comparators and any loading effect.

4.2 Timing Correction

Run the prop delay test function and read the value, compare it to your scope reading and enter the difference in the SATR. Repeat the test and verify that your reading difference is now close to zero.

5. Conclusion

By following carefully through this procedure you can quantify and rule out your interfacing errors and reduce your systematic measurement error terms. Typically you can achieve good correlation down to 150 to 200ps.

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